## AMENDMENTS TO THE SPECIFICATION

Please replace the abstract of the original specification with the following new abstract:

A monolithic three dimensional memory array is described. The memory array comprises a first set of strips including a first terminal; a second set of strips including a second terminal; a third set of strips including a third terminal; a first pillar having at least one side wall with a slightly positive slope, said pillar disposed between and connecting said first and second sets of strips, and including a first P doped silicon region, a first N doped silicon region and a first insulating region; a second pillar having at least one side wall with a slightly positive slope, said pillar disposed between and connecting said second and third sets of strips, and including a second P doped silicon region, a second N doped silicon region and a second insulating region; wherein each of the pillars is substantially free of stringers.



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